What is claimed is:

1. A level conversion circuit comprising:

a first circuit including a first input terminal for receiving a first signal having a first signal amplitude, a first output terminal for supplying a second signal having a second signal amplitude greater than said first signal amplitude and being in the same phase as said first signal, and a second output terminal for supplying a third signal having a second signal amplitude greater than said first signal amplitude and being in the phase reverse to said first signal; and

a second circuit including a first p-channel type MOS transistor, a second p-channel type MOS transistor, a first n-channel type MOS transistor and a second n-channel type MOS transistor whose source-drain routes are connected in series between a first voltage terminal and a second voltage terminal, and the drain of said first p-channel type MOS transistor and the drain of said n-channel type MOS transistor are connected to a third output terminal,

wherein said second circuit forms a fourth signal having said second signal amplitude on the basis of the signal variation of said second signal supplied from said first output terminal of said first circuit or of said third signal supplied from said second output terminal of said first circuit, whichever is faster in signal level change, and supplying said

fourth signal from said third output terminal.

2. A level conversion circuit according to Claim 1, further comprising a delay means for delaying said second signal supplied from said first output terminal of said first circuit or said third signal supplied from said second output terminal of said first circuit to control said second p-channel type MOS transistor and said first n-channel type MOS transistor, or said first p-channel type MOS transistor and said second n-channel type MOS transistor.

3. A level conversion circuit according to Claim 1, wherein a circuit from which, according to a signal inputted to the gate terminal of a MOS transistor, a signal matching said gate input signal is supplied to the source or drain terminal of the MOS transistor is defined to be one stage, the number of circuit stages which a signal reaching said third output terminal of said second circuit from said first input terminal of said first circuit via said second output terminal goes through and the number of circuit stages which a signal reaching said third output terminal of said second circuit from said first input terminal of said first circuit via said third output terminal goes through are equal.

4. A level conversion circuit according to Claim 1, wherein the state of said second p-channel type MOS transistor or first n-channel type MOS transistor in said second circuit varies with change in said second signal or third signal

supplied from said first circuit.

5. A level conversion circuit according to Claim 1 or 4, wherein a high resistance element for pull-up use and a high resistance element for pull-down use are connected respectively in parallel to said first p-channel type MOS transistor and said second n-channel type MOS transistor.

6. A level conversion circuit according to Claim 1 or 5, wherein the ratio between the gate width and the gate length of said first p-channel type MOS transistor is set to be greater than the ratio between the gate width and the gate length of said second p-channel type MOS transistor, and the ratio between the gate width and the gate length of said second n-channel type MOS transistor is set to be greater than the ratio between the gate width and the gate length of said first n-channel type MOS transistor.

7. A level conversion circuit according to Claim 1, wherein a first inverter for logically inverting said first signal is further provided, said first circuit having a second input terminal for receiving the output signal of said first inverter and being comprised of a third n-channel type MOS transistor and a fourth n-channel type MOS transistor whose gate terminals are connected respectively to said first input terminal and second input terminal, a third p-channel type MOS transistor whose source-drain path is connected in series to said third n-channel type MOS transistor and whose gate terminal

is connected to the drain terminal of said fourth n-channel type MOS transistor, and a fourth p-channel type MOS transistor whose source-drain path is connected in series to said fourth n-channel type MOS transistor and whose gate terminal is connected to the drain terminal of said third n-channel type MOS transistor, said first output terminal being connected to the drain terminal of said fourth n-channel type MOS transistor, said second output terminal being connected to the drain terminal of said third n-channel type MOS transistor, and a second inverter for logically inverting said second signal being connected to said first output terminal.

8. A level conversion circuit according to Claim 7, wherein the state of said second p-channel type MOS transistor or first n-channel type MOS transistor in said second circuit varies with change in said second signal or the output signal of said second inverter, whichever is faster in signal variation.

9. A level conversion circuit according to Claim 8, further comprising a third inverter to control said first p-channel type MOS transistor and second n-channel type MOS transistor according to the second signal supplied from said first output terminal of said first circuit or the output signal of said second inverter, whichever is slower in signal variation.

10. A level conversion circuit according to Claim 1,

further having a delay means to control said second p-channel type MOS transistor and first n-channel type MOS transistor or said first p-channel type MOS transistor and second n-channel type MOS transistor according to the signal variation of said second signal supplied from the first output terminal of said first circuit or of said third signal supplied from said second output terminal of said first circuit, whichever is slower in signal variation.

11. A level conversion circuit, according to Claim 1, wherein the state of said first p-channel type MOS transistor or second n-channel type MOS transistor in said second circuit varies in response to a variation of said second signal or third signal supplied from said first circuit, whichever is faster.

12. A level conversion circuit comprising a first circuit including a first input terminal for receiving a first signal having a first signal amplitude, a first output terminal for supplying a second signal having a second signal amplitude greater than said first signal amplitude and being in the same phase as said first signal, and a second output terminal for supplying a third signal having a second signal amplitude greater than said first signal amplitude and being in the phase reverse to said first signal; and

a second circuit for forming a fourth signal having said second signal amplitude on the basis of a variation of said second signal supplied from said first output terminal of said

first circuit or of said third signal supplied from said second output terminal of said first circuit, whichever is faster in signal level change, and supplying said fourth signal from said third output terminal,

wherein said second circuit receives said second signal or third signal supplied from said first circuit and a signal in the reverse phase thereto, and the logical threshold is varied so as to accelerate the variation of said fourth signal according to the direction of signal variation.

13. A level conversion circuit according to Claim 12, wherein said second circuit has a first p-channel type MOS transistor, a second p-channel type MOS transistor, a first n-channel type MOS transistor and a second n-channel type MOS transistor whose source-drain paths are connected in series between a first voltage terminal and a second voltage terminal, the drain of said first p-channel type MOS transistor and the drain of said first n-channel type MOS transistor are connected to said third output terminal, high resistance elements are connected respectively in parallel to said second p-channel type MOS transistor and said first n-channel type MOS transistor, and a delay means is provided to delay said second signal supplied from said first output terminal of said first circuit or said third signal supplied from said second output terminal of said first circuit to control said second p-channel type MOS transistor and first n-channel type MOS transistor or said first

p-channel type MOS transistor and the second n-channel type MOS transistor.

14. A level conversion circuit comprising a first circuit including a first input terminal for receiving a first signal having a first signal amplitude, a first output terminal for supplying a second signal having a second signal amplitude greater than said first signal amplitude and being in the same phase as said first signal, and a second output terminal for supplying a third signal having a second signal amplitude greater than said first signal amplitude and being in the phase reverse to said first signal; and

a second circuit for forming a fourth signal having said second signal amplitude on the basis of a variation of said second signal supplied from said first output terminal of said first circuit or of said third signal supplied from said second output terminal of said first circuit, whichever is faster in signal level change, and supplying said fourth signal from said third output terminal,

wherein a circuit from which, according to a signal inputted to the gate terminal of a MOS transistor, a signal matching said gate input signal is supplied from the source or drain terminal of the MOS transistor being defined to be one stage, the number of circuit stages which a signal reaching said third output terminal of said second circuit from said first input terminal of said first circuit via said second output

terminal goes through and the number of circuit stages which a signal reaching said third output terminal of said second circuit from said first input terminal of said first circuit via said third output terminal goes through are not more than four each.

15. A level conversion circuit comprising a first circuit including a first input terminal for receiving a first signal having a first signal amplitude, a first output terminal for supplying a second signal having a second signal amplitude greater than said first signal amplitude and being in the same phase as said first signal, and a second output terminal for supplying a third signal having a second signal amplitude greater than said first signal amplitude and being in the phase reverse to said first signal; and

a second circuit for forming a fourth signal having said second signal amplitude on the basis of a variation of said second signal supplied from said first output terminal of said first circuit or of said third signal supplied from said second output terminal of said first circuit, whichever is faster in signal level change, and supplying said fourth signal from said third output terminal,

wherein a circuit from which, according to a signal inputted to the gate terminal of a MOS transistor, a signal matching said gate input signal is supplied from the source or drain terminal of the MOS transistor being defined to be one

stage, the number of circuit stages which a signal reaching said third output terminal of said second circuit from said first input terminal of said first circuit via said second output terminal goes through and the number of circuit stages which a signal reaching said third output terminal of said second circuit from said first input terminal of said first circuit via said third output terminal goes through are three each.

16. A level conversion circuit according to Claim 1 to 15,

wherein signals are transmitted in a first amplitude in internal circuits and signals are transmitted and received to and from other external devices in a second amplitude greater than said first amplitude, said level conversion circuit being included in an input circuit or an output circuit of a semiconductor integrated circuit, said input or output circuit being connected to an external terminal at which signals of said second amplitude are supplied.

17. A level conversion circuit according to Claim 16, further comprising, in said input or output circuit connected to said external terminal to which the signals of said second amplitude are inputted, an inverse level conversion circuit for converting signals of said second amplitude into signals of said first amplitude.

18. A semiconductor integrated circuit comprising:

a first level conversion circuit provided with a first

circuit including a first input terminal for receiving a first signal having a first signal amplitude, a first output terminal for supplying a second signal having a second signal amplitude greater than said first signal amplitude and being in the same phase as said first signal, and a second output terminal for supplying a third signal having a second signal amplitude greater than said first signal amplitude and being in the phase reverse to said first signal; and a second circuit for forming a fourth signal having said second signal amplitude on the basis of a variation of said second signal supplied from said first output terminal of said first circuit or of said third signal supplied from said second output terminal of said first circuit, whichever is faster in signal level change, and supplying said fourth signal from said third output terminal; and

a second level conversion circuit comprised of a circuit of the same form as said first circuit.

19. A semiconductor integrated circuit according to Claim 18, wherein said first level conversion circuit is provided on the path of transmitting usual operational signals and said second level conversion circuit, on the path of transmitting testing signals.